BotBlox

BB-AN-0004

UbiSwitch Custom Baseboard Design

Application Note

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BotBlox

Contents

1 Introduction

Designing a custom baseboard for the UbiSwitch module requires a certain level of attention to detail due to the number of signals on the stacking header, and the use of 10Gbps ethernet signals. This application note aims to help the end user design a compliant baseboard for the UbiSwitch Module that will work, first time.

Please refer to the UbiSwitch Baseboard files that are available at the link below.

https://github.com/botblox/UbiConn-BaseBoard-Public

2 Power

The datasheet for the UbiSwitch Module details the specific pins available on the ERM8-030-02.0-S-DV-TR stacking headers. Below is more information on the specific groups of these pins

2.1 Ground pins

Due to the lack of ethernet transformers on UbiSwitch, there is only a single ground on the UbiSwitch Module, which is connected to all ground pins on the stacking header. When using transformers on the baseboard, the user may decide to use a separate ground on the field side of the transformers that is galvanically isolated from the ground used to power UbiSwitch. This is not required in all applications and typically most applications do not require isolated grounds. UbiSwitch is designed to operate directly from a power rail that is noisy and unfiltered.

2.2 VBus Pins

Power is supplied to UbiSwitch via the VBus pins, which expects a 5 to 60V input. This wide voltage range is designed to provide design flexibility on the baseboard, however it should be noted that there is no overvoltage or reverse polarity protection on the VBUS pins. Thus the designer must ensure that this voltage rail will not be subject to…

- Reverse polarity
- Overvoltage exceeding 65V

Ensure that your power supply for UbiSwitch can supply at least 6W to the device.

2.3 3.3V Pin

UbiSwitch generates a 3.3V rail internally, which can be accessed on the stacking header. The maximum current draw from this rail should be limited to 100mA. We do not recommend using this 3.3V rail for anything other than a power status LED on the baseboard.

UbiSwitch will consume a maximum of 4.6W during operation

3 IO and Control

3.1 SE_SCLK

Pin 4 on UbiSwitch is the Synchronous Ethernet input clock for UbiSwitch. A 1.5V, 25MHZ reference clock can be input to this pin to be used as a synchronous clock input for the board. This signal must come from a high quality clock conditioning circuit or Synchronous Ethernet PLL. Note, this signal is not AC coupled, it swings from 0V to 1.5V.

Each PHY, via a PHY register, can select this clock input as its reference clock input instead of using the default XTAL_IN input.

SE_SCLK is internally pulled low via a resistor so the pin can be left floating when unused.

There is already a high quality 25MHz oscillator on UbiSwitch, so unless your application specifically requires Synchronous Ethernet (most applications do not), we recommend leaving this pin unconnected.

Please note, if you do need to use synchronous ethernet, you will need to configure the firmware running on UbiSwitch. Please get in touch with us if this is the case.

Table 1 below shows the electrical parameters required for the Synchronous Ethernet Clock.

Symbol	Parameter	Min	Typical	Max	Unit
V_{IL}	Low level input voltage	-0.3	-	0.54	V
V_{IH}	High level input voltage	1.4	-	1.99	V
T_p	Clock Period	40 - 50ppm	40	40 + 50ppm	ns
T_H	Clock High Time	13	20	27	ns
T_L	Clock Low Time	13	20	27	ns
T_R	Clock Rise Time	-	-	3	ns
T_F	Clock Low Time	-	-	3	ns

T_F	Clock total jitter	-	-	200	ps*

**Broadband peak-peak = 200ps, Broadband rms = 3ps, 12 KHz to 20MHz = 1ps*

Table 1: Input voltage logic thresholds for SE_SCLK

3.2 SMI (MDIO_CPU and MDC_CPU)

These pins allow direct access to the SMI bus that can be used to configure the behavior of the ethernet switch onboard UbiSwitch. We do not recommend connecting any active device to these pins unless you expect to be writing your own firmware for configuring the switch.

For most baseboard designs, we recommend simply connecting these pins to test points on your baseboard, just in case the internal configuration bus needs to be debugged at a later date.

Note, be careful when routing out these signals to test points; you want to avoid these test points acting like antennae, and thus picking up noise. Do not exceed a length of 50mm on these lines. If you intend to route these pins further than this, or connect to a multidrop SMI bus, we recommend placing a simple line driver on the MDIO and MDC lines. An example of such a line driver that would work is the NL17SZ125DBVT1G from OnSemi.

The SMI signals are simple 3.3V signals which utilize the input level thresholds in the table below. You do not need external pull up resistors on these signals.

Symbol	**Parameter**	**Min**	**Max**
V_{IL}	Low level input voltage	-0.4V	0.99V
V_{IH}	High level input voltage	2.3V	3.7V

Table 2: Input voltage logic thresholds for SMI pins on UbiSwitch

3.3 Eth_RST

This is the reset pin for UbiSwitch. UbiSwitch contains power rail sequencing and reset, so you should not need to actively control the reset line on your baseboard. In most applications, you can simply break this pin out to a test point in case it is necessary for testing. Note, be careful when routing out these signals to test points; you want to avoid these test points acting like antennae, and thus picking up noise. Do not exceed a length of 50mm on these lines.

This signal is a 3.3V level, active low signal. Pull the signal low to reset UbiSwitch.

Symbol	Parameter	Min	Max
V_{IL}	Low level input voltage	-0.4V	0.99V
V_{IH}	High level input voltage	2.3V	3.7V

Table 3: Input voltage logic thresholds for reset pin on UbiSwitch

3.4 USART_RX and USART_TX

These pins connect to the serial port of the microcontroller on board UbiSwitch, and allow serial commands to be sent to/from the microcontroller for configuring UbiSwitch. This is the recommended way for configuring UbiSwitch. These pins are 3.3V level logic and do not require any external pull up or pull down resistors.

If you expect access some of the switch management functions on UbiSwitch, we recommend breaking out these pins and connecting them to either a microcontroller on your baseboard, or to a connector on your baseboard that can later be connected to the device that will be sending serial commands to UbiSwitch.

The voltage levels for these pins can be shown below. If you expect to be routing these signals a long distance (exceeding 500mm), we recommend placing simple line drivers (eg NL17SZ125DBVT1G) on these lines.

Symbol	Parameter	Min	Max
V_{IL}	Low level input voltage	-	1.23V
V_{IH}	High level input voltage	1.88V	-

Table 4: Input voltage logic thresholds for UART pins on UbiSwitch

For the purposes of serial communication, the baud rate of the serial connection will be 115200 baud.

3.5 LED Signals

The port indication LEDs on UbiSwitch do not provide a dedicated signal for each port. Instead, the signals are multiplexed, and thus must be connected to a specific matrix arrangement of LEDs. Figure 1 below shows an example circuit for this.

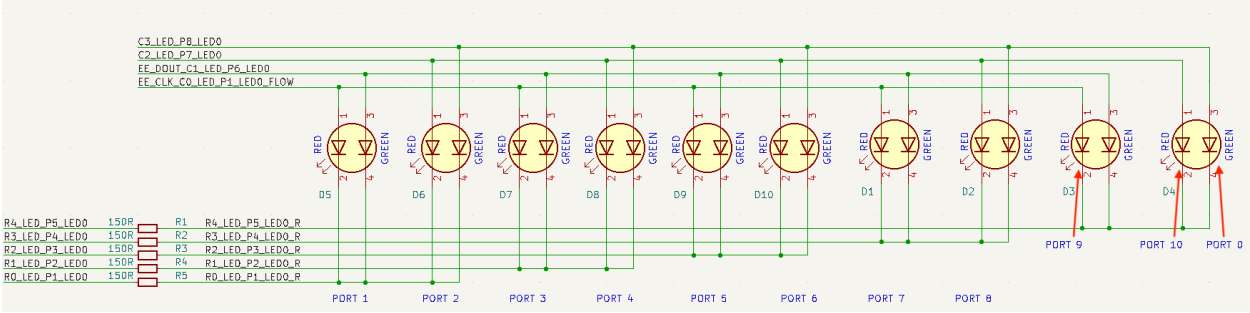

Figure 1 - Port LED indicators

Ports 1 to 8 use two LED signals to indicate link speed and activity. In figure 14 above, these two LED signals are mapped to a dual color LED, but this could alternatively be two single color LEDs. In figure 1 above, the color corresponds to the link speed and activity is shown via blinking. (Green blinking indicates a 1000 Mbps connection, Red blinking indicates a 100Mbps connection, Orange blink indicates a 10Mbps connection). A solid on LED indicates Link/No Activity.

The voltage levels for these signals is shown in table 5 below.

Symbol	Parameter	Min	Max
V_{OL}	Low level output voltage	-	0.4V
V_{OH}	High level input voltage	2.9V (I_{OH} = -7mA)	-

Table 5: Input voltage logic thresholds for UART pins on UbiSwitch.

Figure 1 below shows an example circuit with 150 Ohm resistors for limiting current in the LEDs. You may wish to slightly change the value of this resistor based on the desired brightness of the LED used in your design.

4 1GBASE-T Ports

There are 8 1GBASE-T ports on UbiSwitch that can operate in 10BASE-T, 100BASE-TX and 1000BASE-T modes of operation.

4.1 Auto negotiation

All 8 1GBASE-T ports support auto negotiation and will automatically negotiate with any connected device to achieve the highest possible link speed based on the connected device's capabilities. This is the default configuration of these ports on UbiSwitch. Auto negotiation can be disabled through switch configuration, and the port can be fixed to a particular speed. In

most cases it is not advisable to do this since it is simpler to just let the auto negotiation protocol handle any differences in port capabilities.

4.2 Auto MDI/X

The 8 ports support Auto-MDI/X by default, meaning the ports will automatically determine whether or not they need to cross over between its pairs as shown in table 6. This means that an external crossover cable is not required when using these ports.

Pin	**MDI**			**MDIX**		
	1000BASE-T	100BASE-TX	10BASE-T	1000BASE-T	100BASE-TX	10BASE-T
MDIP/N[0]	BI_DA±	TX±	TX±	BI_DB±	RX±	RX±
MDIP/N[1]	BI_DB±	RX±	RX±	BI_DA±	TX±	TX±
MDIP/N[2]	BI_DC±	Unused	Unused	BI_DD±	Unused	Unused
MDIP/N[3]	BI_DD±	Unused	Unused	BI_DC±	Unused	Unused

Table 6: MDI/MDIX Pin Mapping

If a connected device cannot automatically correct for crossover the ports on UbiSwitch will make the necessary adjustments prior to commencing auto negotiation. If a connected device can automatically correct for crossover, UbiSwitch will implement a random algorithm as described in IEEE 802.3 clause 40.4.4 to determine which device performs the crossover. This feature can be disabled through switch configuration, however this is not advised.

This means you do not necessarily have to worry about getting TX and RX the correct way round for 100BASE-TX or 10BASE-T ethernet. However in general it is always good design practice to rout the signals as cross cables (TX on UbiSwitch to RX on the connected device).

4.3 Polarity Correction

UbiSwitch will automatically correct polarity (+ and - wiring mistakes) errors in the receive connections in 1000BASE-T and 10BASE-T. In 100BASE-TX, the polarity does not matter. This allows UbiSwitch to compensate for an incorrect polarity.

You can make use of this fact in your baseboard design to swap over polarities to ease routing constraints.

5 10G MAC Ports

Ports 0, 9 and 10 on UbiSwitch are SERDES interfaces that implement MAC ports on the switch. These are different to the 8 x 1G ports described above, because they are not capable of being directly connected to an external system by themselves. They require a physical layer transceiver (PHY) to be converted from a MAC level interface to a field level interface such as 10GBASE-T (10Gbps on four copper pairs) or 10GBASE-R (10Gbps backplane for connection to SFP. While this may seem like a limitation, this allows flexibility on these ports, as any type of PHY can be connected to them to achieve any type of ethernet media connection.

Ports 9 and 10 can support SGMII, 5GBASE-X, SFI and USXGMII while port 0 can support RGMII, RMII, MII, SGMII, 5GBASE-X, SFI and USXGMII. By default, UbiSwitch configures all these ports to operate in SFI mode as 10GBASE-R, which is the required mode when connecting to an external SFP, as is the case on the UbiConn breakout board.

In this mode, only 10G capable SFPs can be used. 1G SFPs use a SGMII backplane, and thus will not work when these ports are left in their default state. To use 1G SFPs, these ports need to be configured as SGMII. This is only possible through custom firmware on UbiSwitch. We are actively developing a user configuration software for UbiSwitch; once complete it will allow the user to easily configure these ports as SGMII or 10GBASE-R over serial.

Note, you can still achieve a 1G/2.5G/5G connection with most 10G copper SFP. This is because most 10G copper SFPs will support auto negotiation down to lower rates. To achieve this, you will need to set a slower speed on the device connected to the SFP, or simply use a connected device that does not support 10Gbps.

6 Integrating external 10G Copper PHYs

Many applications require the use of 10Gbps copper ports with UbiSwitch. While this is possible by placing an SFP on the USXGMII ports, and then using a 10G Copper SFP (such as this), this is not a space efficient way to achieve this. Instead, a more elegant way is to embed 10GBASE-T Physical Layer Transceivers (PHYs) directly onto your baseboard.

If you want to achieve this in your application, please get in touch with us for information.

7 PCB Requirements

7.1 PCB and stackup requirements

To achieve the necessary impedances on the 1G and 10G signals from UbiSwitch Baseboard, we recommend using the following stackable and track thicknesses on your baseboard.

Both the 1GBASE-T ports and the 10G USXGMII ports use the same track thickness and spacing on UbiSwitch, which is...
Track width = 0.1016mm
Copper thickness = 0.5 oz-in
Clearance between traces in differential pair = 0.11mm
Dielectric = FR-4
Surface treatment = ENIG
Distance above nearest ground place = 0.1016mm

This yields a differential impedance of around 95 Ohm, which is within 10% of the target and generally fine. You can check the impedance of different designs here.

All differential lines in our designs are micro-stripline (either top or bottom layer with a ground plane immediately above/below). We do not use any of the internal layers for the high speed differential lines. If you do, you may need to adjust your track width and spacing to achieve the target 100 Ohm differential impedance.

7.2 Recommended skew

10G USXGMII

- Keep the intra-pair skew to less than 0.1mm (between a + and - of a single pair)
- Keep the inter-pair skew to less than 0.5mm (between a TX and RX in a signal USXGMII port)
- No requirement to tune lengths between different USXGMII ports.

1GBASE-T

- Keep the intra-pair skew to less than 1mm
- Keep the inter-pair skew to less than 0.5mm
- No requirement to tune lengths between different 1GBASE-T ports.

8 Datasheet Changelog

Date	Datasheet Version	Author	Notes
20/07/2023	A_A	Josh Elijah	Initial release
01/08/2023	A_B	Josh Elijah	Fixed mistake that described reset line as an active high signal. It is an active low signal.
14/10/2023	A_C	Josh Elijah	Fixed the incorrectly labeled SFP link indicator signals

9 Contact

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